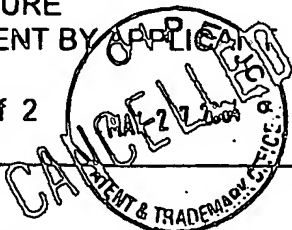


INFORMATION  
DISCLOSURE  
STATEMENT BY APPLICANT

Sheet 1 of 2

Application Number: 10/768,754  
Filing Date: January 26, 2004  
First Named Inventor: Adrian STOICA, et al.  
Group Art Unit: Unknown  
Examiner Name: Unknown  
Attorney Docket Number: NPO-20535-2-CU



Examiner  
Initials

NON PATENT LITERATURE DOCUMENTS

2	BENNETT, F. III, et al. "Evolution of a 60 decibel Op Amp Using Genetic Programming", <i>First Int'l. Conf. On Evolvable Systems</i> , Springer-Verlag, Japan, 1996, pp. 455-469.
3	FLOCKTON, STUART J., et al., "Intrinsic Circuit Evolution Using Programmable Analogue Arrays," <i>Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware</i> , Springer-Verlag, Switzerland, 1998, pp. 144-153.
2	IBA, HITISHI, et al., "Machine Learning Approach to Gate-Level Evolvable Hardware," <i>Proc. Of the First Int'l. Conf. On Evolvable Systems</i> , Springer-Verlag, Japan, 1996, pp. 327-343.
3	KAJITANI, ISAMU, et al., "A gate-level Etw Chip: Implementing GA operations and reconfigurable hardware on a single LSI," <i>Proc. Of the Second Int'l. Conf. On Evolvable Sytems: From Biology to Hardware</i> , Springer-Verlag, Berlin, 1998, pp. 1-12.
3	KOZA, JOHN R., et al., "Reuse, Parameterized Reuse, and Hierarchical Reuse of Substructures in Evolving Electrical Circuits Using Genetic Programming," <i>Proc. Of the First Int'l. Conf. On Evolvable Systems</i> , Springer-Verlag, Japan, 1996, pp. 312-326.
3	KOZA, JOHN R., et al., "Automated WYWIWYG Design of Both the Topology and Component Values of Electrical Circuitis Using Genetic Programming," <i>Proc. Of the First Annual Genetic Programming Conference</i> , MIT Press, Cambridge MA, 1996, pp. 123-131.
3	KOZA, JOHN R. et al., "Automated Synthesis of Analog Electrical Circuits by Means of Genetic Programming," <i>IEEE Transaction on Evolutionary Computation</i> , Vol. 1, No. 2, 1997, pp. 109-128.
2	LOHN, JASON D., et al., "Automated Analog Circuit Synthesis Using a Linear Representation," <i>Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware</i> , Springer-Verlag, Berlin, 1998, pp. 125-133.
3	MURAKAWA, MASAHIRO, et al., "Analogue EHW Chip for Intermediate Frequency Filters," <i>Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware</i> , Springer-Verlag, Berlin, 1998, pp. 143-143.
3	STOICA, ADRIAN, "On Hardware Evolvability and Levels of Granularity," <i>International Conference On Intelligent Systems and Semiotics</i> , NIST, Gaithersburg VA, September 1997, pp. 244-247.
2	THOMPSON, ADRIAN, "Silicon Evolution," <i>Proc. Of the First Annual Genetic Programming Conference</i> , MIT Press, Cambridge MA, 1996, pp. 444-452.
3	THOMPSON, ADRIAN, "On the Automatic Design of Robust Electronics Through Artificial Evolution," <i>Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware</i> , Springer-Verlag, Switzerland, 1998, pp. 13-24.
3	THOMPSON, ADRIAN, "An evolved circuit, intrinsic in silicon, entwined with physics," <i>Proc. Of the First Int'l. Conf. On Evolvable Systems</i> , Springer-Verlag, Japan, 1996, pp. 390-405.


Examiner's Signature:

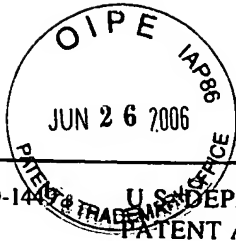
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Date Considered:

*6/5/06*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  Sheet 2 of 2		Application Number: 10/768,754 Filing Date: January 26, 2004 First Named Inventor: Adrian STOICA, et al. Group Art Unit: Unknown Examiner Name: Unknown Attorney Docket Number: NPO-20535-2-CU	
Examiner Initials	NON PATENT LITERATURE DOCUMENTS		
3	ZEBULUM, RICHARD S., et al., "Evolvable Systems in Hardware Design: Taxonomy, Survey and Applications," <i>Proc. Of the First Int'l. Conf. On Evolvable Systems</i> , Springer-Verlag, Japan, 1996, pp. 344-358.		
3	ZEBULUM, RICHARD S., et al., "Analog Circuits Evolution in Extrinsic and Intrinsic Modes," <i>Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware</i> , Springer-Verlag, Berlin, 1998, pp. 154-165.		
Examiner's Signature: 		Date Considered: 6/5/04	
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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

Attorney Docket No.: NPO-20535-2-CU Serial No.: To be Assigned

Applicant(s): Adrian STOICA, et al.

Filing Date: Herewith

Group: Unknown

**LIST OF PRIOR ART CITED BY APPLICANT**

(Use several sheets if necessary)

**U. S. PATENTS**

Initials	Patent No	Issue Date	Name	Class	Subclass	Filing Date
3	US-5,258,947	11-02-1993	SOURGEN	365	96	12-07-1990
3	US-5,677,691	10-14-07	HOSTICKA ET AL.	341	155	06-25-1993
7	US-5,705,938	01-06-1998	KEAN	326	39	09-05-1995
3	US-5,867,397	02-02-1999	KOZA ET AL.	364	489	02-20-1996
3	US-5,897,628	04-27-1999	KITANO	706	13	09-10-1996
3	US-5,959,871	09-28-1999	PIERZCHALA ET AL.	364	489	12-22-1994
3	US-5,970,487	10-19-1999	SHACKLEFORD ET AL.	707	6	08-13-1997
3	US-6,360,191	03-19-2002	KOZA ET AL.	703	6	01-05-1999
3	US-6,363,517	03-26-2002	LEVI ET AL.	716	16	06-17-1999
3	US-6,363,519	03-26-2002	LEVI ET AL.	716	16	06-17-1999
3	US-6,378,122	04-23-2002	LEVI ET AL.	716	16	06-17-1999

**FOREIGN PATENT DOCUMENTS**

Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials

Other Documents (Title, Author, Date, Pages, Etc., if known)

Augusto, Soares J.A., and Almeida, Beltran C.F., "Analog Fault Diagnosis in Nonlinear DC Circuits with an Evolutionary Algorithm," *IEEE*, July 2000, pp. 609-616.Layzell, Paul, "A New Research Tool for Intrinsic Hardware Evolution," Second International Conference, *ICES98*, Lausanne, Switzerland, Springer, September 23-25, 1998, pp. 47-56.Examiner's Signature: 

Date Considered: 6/5/04

Initial if reference was considered, whether or not citation with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).

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Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials

Other Documents (Title, Author, Date, Pages, Etc., if known)

Perkowski, M. Chebotarev, A., and Mishchenko, A., "Evolvable Hardware or Learning Hardware? Induction of State Machines from Temporal Logic Constraints," *Proceedings of the First NASA/DoD Workshop*, July 19-21, 1999, pp. 129-138.

Stoica, Adrian, "Reconfigurable Transistor Arrays for Evolvable Hardware," NASA Tech Brief, Vol. 25, No. 2, Item # from JPL New Technology Report NPO-20078, July 26, 1996, pp5a.

Stoica, Adrian, "Evolvable Hardware: From On-Chip Circuit Synthesis to Evolvable Space," *IEEE*, May 2000, pp. 1-9.

Stoica, Adrian, "Toward Evolvable Hardware Chips: Experiments with a Programmable Transistor Array," *IEEE*, April, 1999, pp. 1-7.

Stoica, A., Keymeulen, D., Duong, V., and Salazar-Lazaro, C., "Automatic Synthesis and Fault-Tolerant Experiments on an Evolvable Hardware Platform," *IEEE*, October 2000, pp. 465-471.

Stoica, A., Keymeulen, D., Salazar-Lazaro, C., Li, W., Hayworth, K., and Tawerl, R., "Toward On-board Synthesis and Adaption of Electric Functions: An Evolvable Hardware Approach," *IEEE*, Vol. 2, March, 1999, pp. 351-357.

Stoica, A., Keymeulen, D., Tawel, R., Salazar-Lazaro, C., and Li, W., "Evolutionary experiments with a fine-grained reconfigurable architecture for analog and digital CMOS circuits," *Evolvable Hardware '99: Proceedings of the First NASA/DoD Workshop on Evolvable Hardware*, Pasadena, CA, July 19-21, 1999.

Stoica, A., Salazar-Lazaro, C., and Tawel, R., "Evolvable Electronic Systems," *1998 Military and Aerospace Applications of Programmable Devices and Technologies (MAPLD) Conference*, Pasadena, CA, September 15-16, 1998.

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Attorney Docket No.: NPO-20535-2-CU Serial No.: To be Assigned

Applicant(s): Adrian STOICA, et al.

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Group: Unknown

**LIST OF PRIOR ART CITED BY APPLICANT***(Use several sheets if necessary)***U. S. PATENTS**

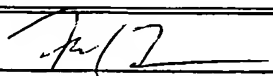
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**FOREIGN PATENT DOCUMENTS**

Initials	Document Number	Date	Country	Name	Translation? (Yes/No/n/a)

Initials	Other Documents (Title, Author, Date, Pages, Etc., if known)
2	Stoica, A., Keymeulen, D., Zebulum, R., Thakoor, A., Daud, T., Klimeck, G., Jin, Y., Tawel, R., and Duong, V., "Evolution of analog circuits on Field Programmable Transistor Arrays," <i>IEEE</i> , July, 2000, pp. 1-10.
3	Stoica, A., Klimeck, G., Salazar-Lazaro, C., Keymeulen, D., and Thakoor, A., "Evolutionary Design of Electronic Devices and Circuits," <i>Evolutionary Computation, Proceedings of the 1999 Congress</i> , Washington, D.C., July 6-9, 1999, pp. 1271-1278.
3	Zebulum, R., Pacheco, M., "Evolvable Hardware: On the Automatic Synthesis of Analog Control Systems," <i>IEEE</i> , March, 2000, pp. 451-463.
2	Zebulum, R., Stoica, A., and Keymeulen, D., "A Flexible Model of a CMOS Field Programmable Transistor Array Targeted for Hardware Evolution," <i>3<sup>rd</sup> International Conference of Evolvable Systems, ICES2000</i> , Edinburgh, Scotland, April, 2000.

Examiner's Signature:



Date Considered:

6/5/00

Initial if reference was considered, whether or not citation with MPEP. Mark through citation if not considered. Include a copy of this citation form with your next correspondence to the Applicant(s).

**Notice of References Cited**

Application/Control No.

10/768,754

Applicant(s)/Patent Under  
Reexamination  
STOICA ET AL.

Examiner

Fred Ferris

Art Unit

2128

Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,363,519	03-2002	Levi et al.	716/16
*	B	US-6,363,517	03-2002	Levi et al.	716/6
*	C	US-5,970,487	10-1999	Shackleford et al.	707/6
*	D	US-5,677,691	10-1997	Hosticka et al.	341/155
*	E	US-5,021,856	06-1991	Wheaton, Larry B.	257/565
*	F	US-6,360,191	03-2002	Koza et al.	703/6
*	G	US-5,867,397 A	02-1999	Koza et al.	703/14
*	H	US-6,094,065 A	07-2000	Tavana et al.	326/39
*	I	US-6,526,556 B1	02-2003	Stoica et al.	716/16
*	J	US-6,378,122 B1	04-2002	Levi et al.	716/16
*	K	US-6,195,593 B1	02-2001	Nguyen, Son Ngoc	700/97
*	L	US-6,728,666 B1	04-2004	Stoica et al.	703/13
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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